Noname manuscript No.
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An Overview of Model Checking Practices on Verification of PLC Software

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Received: / Accepted:

Abstract Programmable Logic Controllers (PLC) are heavily used in industrial control systems, because of their high capacity of simultaneous input/output processing capabilities. Characteristically, PLC systems are used in mission critical systems and PLC software need to conform real time constraints in order to work properly. Since PLC programming requires mastering low level instructions or assembly-like languages, an important step in PLC software production is modeling using a formal approach like Petri nets or automata. Afterwards, PLC software is produced semi-automatically from the model and refined iteratively. Model checking, on the other hand, is a well-known software verification approach, where typically a set of timed properties are verified by exploring the transition system produced form the software model at hand. Naturally, model checking is applied in a variety of ways to verify the correct-

This study is supported by The Scientific and Technological Research Council of Turkey within the project numbered 113E272

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ness of PLC based software. In this paper, we provide a broad view about the difficulties which are encountered during the model checking process applied at verification phase of PLC software production. We classify the approaches from two different perspectives: first the model checking approach/tool used in the verification process, and second the software model/source code and its transformation to model checker's specification language. In a nutshell, we have mainly examined SPIN, SMV and UPPAAL based model checking activities and model construction using instruction lists (IL) (and alike), Function Block Diagrams (FBD) and Petri nets/automata based model construction activities. As a result of our studies, we provide a comparison among the studies in the literature regarding various aspects like their application areas, performance considerations and model checking processes. Our survey can be used to provide guidance for the scholars and practitioners planning to integrate model checking to PLC based software verification activities.

Keywords Model Checking · Programmable Logic Controllers · Program Verification

1 Introduction

Programmable Logic Controllers (PLCs) can be seen as special kind of computers which are capable of processing a high number of I/O operations conforming real time constraints. A typical PLC's processing cycle is arranged in three distinct sections where the input data is read into memory, data in the memory is processed and the output data is written. The essence in widespread usage of PLCs is the limited duration of this cycle where input processing and production of outputs should be produced in hard deadlines. This situation makes PLCs a key artifact in real-time automation and control processes like railway interlocking systems (Pavlovic and Ehrich, 2010) (Enoiu et al, 2013b), nuclear power plants (Jeon, 2007) (Jee et al, 2010) (Yoo et al, 2008), manufacturing conveyors (Couffin and Lesage, 2000), (Klein et al, 2002), etc.

Being a digital computer, a PLC needs to be programmed in order to serve different purposes in different areas of usage. Tremendous increase in the utilization of PLCs in the last decades has also risen the number of PLC manufacturers and hence the variety in programming/modeling aspects. During the development of PLC programming, the industry has gone a series of evolutions in program specification and the programming language to be used, forming an industry standard called IEC 61131 (John and Tiegelkamp, 2010). A part of this standard defines common programming elements like variables and data types for a total of four programming languages in an either graphical or textual format. Most of the tools and practices in today's PLC programming activities are based on these programming languages, namely: Instruction Lists (IL), Structured Texts (ST), Function Block Diagrams (FBD) and Ladder Diagrams (LD).

With respect to conventional computer programming techniques, PLC programming is performed in low level programming languages where bitwise

operations and Boolean variables are frequently used. This situation makes understanding and debugging of PLC programs inherently hard, increasing the importance of testing and verification of PLC programs. Even more importantly, PLCs are mostly used in mission critical real time systems where the flaws in the complete correctness of the system software generally lead to produce hazardous effects. These two aspects combined make it very important to verify the correctness of PLC software in a rigorous manner.

The intense need for the verification of PLC software has given formal methods a key aspect in this area for two main reasons. Firstly, because of the mathematical rigor behind the formal methods, it is able to provide proofs for the correctness of software/model under consideration. Secondly, it is possible to apply formal methods on different levels of abstractions of the target system, which makes it possible to work on early stages of the software design. This property of formal methods is useful since it is known that the most serious (and hard to fix) software defects are known to arise at the early design stage of software production. The two prominent methods in formal verification are known to be theorem proving and model checking. These methods are applied in a large context in PLC software verification, however we will be focusing on model checking practices in this paper's context.

Model checking is a widely used formal method where the system to be verified is represented by a suitable model and the desired property to be verified is checked by systematically exploring all the possible states that the modeled system may go through in a brute-force manner. By considering all possible scenarios the verified property can be guaranteed depending on the correctness of the system model. For instance, a common model checking practice is to build the model using a state transition system and to specify the temporal properties of the system using Linear Temporal Logic(LTL) (Pnueli, 1977). This way, the automated model checking process can be applied by performing an exhaustive state space search over the multiplication of the transition system and the temporal specification to be checked. The transition system used in model checking is constructed by parallel composition of software/hardware component models.

Model checking is specifically useful when it comes to the verification of PLC systems, because it can be easier to model low level PLC software as state transition systems compared to conventional computer programming. Moreover, since the PLC programs needs to be transferred frequently among different PLC hardware, modeling takes an important place in PLC programming in abstracting away unnecessary details. Even more, standard graphical languages like Function Block Diagrams (FBDs) or Sequential Function Charts (SFCs) (John and Tiegelkamp, 2010) and widely accepted modeling languages like Petri nets (Peterson, 1981) have the potential to be translated to transitions systems more easily.

Following the progress in PLC programming and model checking, a large number of integration studies have been carried out in the related fields during the last decades. Most of these studies were about the translation challenges between formalisms used in PLC programming and a specific model checking

tool. In this paper, we present a broad overview of these studies and summarize the challenges faced in the course. We present a two fold classification in the paper; the main classification groups the studies according to the programming/modeling methodology used in expressing PLC program and the target model checker. A secondary classification for each programming/modeling methodology is also presented where a number of important aspects (e.g. application context, applied system size, performance, automation level) about each study in the class are compared.

For our main classification, we have firstly used the five main programming languages in the IEC 61131-3 standard which are Ladder Diagrams, Instruction Lists, Structured Text, Function Block Diagrams and Sequential Function Charts. In addition to those languages we have also included the studies which use other formalisms, mainly Petri nets as well as PLC-Automata (Dierks, 1997), Condition Event Systems (Sreenivas and Krogh, 1991) and a few others which are explained in Section 3.4. In our main classification, we have also included model checking languages that were used; mainly SMV (McMillan, 1999) (NuSMV, CadanceSMV), Timed Automata (Alur and Dill, 1994) (UPPAAL, Kronos), Promela/SPIN (Holzmann, 1997) and a few others. As a result of this classification, we also aim to reveal, if exists, relations between certain PLC programming languages and model checking methods.

For our secondary classification, we have enlisted some important properties of the studies for each group of PLC programming languages. These properties include application areas, system size, performance evaluation (if any), level of automation and specification representation. By examining the commonalities among these properties we can comment about some certain characteristics of PLC programming languages from the perspective of model checking.

As a result of our classification study, we present important common challenges that are present in the examined studies and discuss future studies that can be fruitful in the research area such as the use of timer-on delays and classical state space explosion problem. Our findings also provide a general overview for the practitioners who wish to apply model checking on a PLC based system. The state-of-the-art application area for model checking PLC programs is transforming programs represented by Functional Block Diagrams(FBDs) to either SMV or UPPAAL models depending on the necessity to consider time explicitly in the model. Our overview gives insight about the type of model checkers used for specific types of PLC programming languages, the size of the system for the model checking to be applied, and the obstacles that may be present during the process.

The rest of the paper is organized as follows; Section 2 provides an overview of the merits and weaknesses of PLC programming compared to conventional programming and Section 3 introduces PLC programming techniques included in the paper. Section 4 begins with the explanation of research methodology and an overview of related surveys in the industrial automation and PLC programming and later present the main classification of the studies that will be covered in the paper. Overview of studies for each group of PLC program-

ming language is presented in Sections 5 to 8 together with the discussion of secondary classification results. We also review recent studies that practically apply PLC model checking on industrial sized systems in Section 9. In Section 10 we present a discussion about the challenges present in the examined papers and clarify some open problems and future challenges. Finally, we conclude the paper in Section 11.

2 PLC Programming

Historically, PLC programming has grown from the roots of ladder diagrams (see Figure 4) almost directly modeling the early usage of relays in control systems (John and Tiegelkamp, 2010). The basic usage principles of ladder diagrams can be used to understand neatly how PLC programming works in general. In ladder diagrams, a series of on/off switches(relays) are used in conjunction and disjunction in order to connect PLC inputs to PLC outputs representing the control logic as a propositional logic formula. In PLC programming inputs and outputs are predefined in PLC hardware making the programming simply a correct selection of inputs/outputs and application of control logic. Roughly comparing to conventional computer programming where a new input/output variable is defined as the program code evolves, PLC programs usually start with a full range of I/O as refinements are continuously applied during the development process.

Another major difference of PLC programming is the execution logic of the PLC program after it has been developed. As mentioned earlier, PLC programs follow a "'read input"' - "'execute logic"' - "'update outputs"' approach, which results in the re-execution of the PLC program in each execution cycle. In terms of execution, PLC programs are prepared under an inherent parallel execution approach, because of their basis in electrical control circuits. For instance in ladder diagrams, each relay lane (which is also called a rung) is executed in parallel. This execution approach and the large number of I/O makes PLC programs undesirably large and complicated making them very hard to debug and maintain.

There are approaches like Sequential Function Charts(see Section 3.3.1) that can be used to abstract away subsections of ladder diagrams as blocks to provide a perspective to the overall PLC program. However, too much abstraction can be undesired for PLC programs since it can make the PLC program even harder to maintain during system failures. The main usage are of PLCs and PLC programs are manufacturing, conveyor systems and critical systems like power plants making long downtimes unacceptable. This situation brings up the preference of large program size and under-abstraction rather than longer debugging and maintenance durations.

All of the characteristics of PLC programming discussed above makes it an appropriate application area for model checking, because of the following 3 reasons: i) The program logic of PLC programs can be easily transformed to propositional logic and state transition systems ii) PLC programs inherently

run parallel iii) PLC programs are mostly used in real-time systems making verification a more important issue. There also exists more recent techniques than Ladder diagrams and sequential function charts in PLC programming, we enlist and examine them in the following section.

3 PLC Program Models

Among model checking practices in the area of PLC software, our main interest is the program code/model that was used as the main artifact when performing the translation to the modeling language of the model checker. During this translation process, PLC program models are also used as a basis in large number of studies instead of PLC program code. In these studies, PLC programs are generated either manually or automatically, however translation to the model checking language is done using the models. For this reason, we also include a few modeling languages to our classification in addition to the standard PLC programming languages.

In the industry standard IEC 61131-3, two main groups of programming languages are included, namely textual programming languages and graphical programming languages. Our classification is mainly based on this definition, however there also exist higher level of graphical modeling languages which provide more abstract models for the organization of PLC programs. One of those languages is Sequential Function Charts (SFC) which structure the internal organization of a control program, treating blocks of PLC program as components. SFCs are also included in IEC 61131-3 standard providing a step of higher level modeling to programming languages defined in the standard. Having a strong formal basis and allowing concurrent execution modeling, Petri nets are another modeling language frequently used in the modeling of PLC programs.

Together with the mentioned PLC programming standards we also treat SFCs and Petri nets as a separate class of studies in Model Checking PLC programs since there exists a large number of studies using these modeling languages as basis. In this section, we continue by giving brief overviews of these languages since we will be frequently mentioning properties of them through the remainder of the paper. In addition to these 6 categories, there are also some other studies which we aggregate into a distinct group including non-conventional ways of PLC program specification. We explain those studies in more detail in Section 3.4.

3.1 Text Based Programming Languages

The two text based models introduced in the industry standard are Instruction Lists (IL) and Structured Texts (ST). Both of these programming languages resemble conventional low level programming languages and take their roots from the very early days of PLC technology.

```
          LD      Speed
          GT      1000
          JMPCN   VOLTS_OK
          LD      Volts
VOLTS_OK  LD      1
          ST      %Q75
```

Fig. 1 An example PLC program snippet written in Instruction List (Lewis, 1998)

```
IF Speed > 1000 Then
  Volts := Volts - 10;
END_IF;
%Q75 := 1;
```

Fig. 2 An example PLC program snippet written in Structured Text (equivalent of Figure 1)

Instruction Lists are the primary means of PLC programming similar to an assembly language in syntax. Instructions in the IL are imperative operations which may have parameters and use registers to store values. IL programs also use the very basic components of the PLC hardware during its operations. IL is very frequently used in translation to model checking languages since almost any other programming language used in PLC programming can be converted to IL programs. An example IL program can be seen in Figure 1.

Structured Lists, on the other hand, take its roots from Pascal programming language allowing conditional and iteration statements included in the programs. Those kind of functionality can be realized by using jump statements in IL. Structured Text also defines a more convenient syntax for defining functions and function blocks forming a higher level language when compared to IL. An example Structured Text program can be seen in Figure 2.

3.2 Graphical Programming Languages

3.2.1 Function Block Diagrams

Function blocks are defined as the equivalent of integrated circuits for the PLC programs. They gather the functions supplied by the PLC to perform a specific functionality. These functions can be elementary blocks performing basic functions like move and compare or composite blocks that were constructed by connecting a set of functions. Having well-defined input and output, function blocks can be used like black boxes by the PLC programmers.

Function Block Diagrams (FBD) are the graphical structures that contain information about how the function blocks inside PLC program is related and how the information is going to flow among them. An example program with Function Block Diagrams can be seen in Figure 3. By their nature, FBDs mimic different levels of abstractions by encapsulating the elementary func-

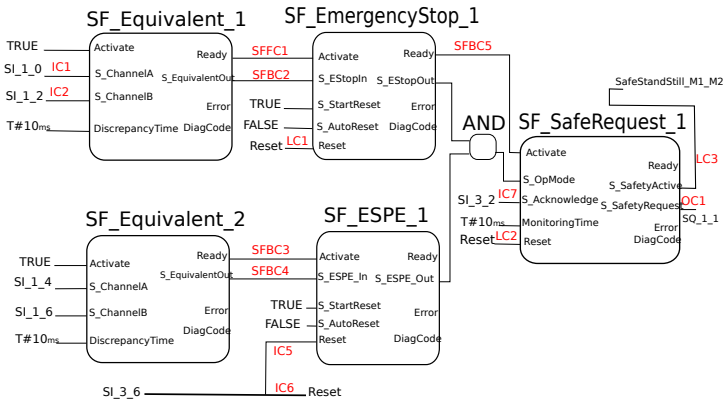

Fig. 3 Function Block Network of a PLC Software (Soliman and Frey, 2011)

tions and interconnected function blocks. This makes FBDs very popular in model checking FBD programs, because reduction of system complexity by applying abstractions is one of the key practices in reducing the state space during model checking process.

3.2.2 Ladder Diagrams

Ladder diagrams, originally used for designing relay racks, has evolved into a programming language for PLC controllers in time. Also expressed as ladder logic or relay ladder logic, ladder diagrams actually are composed of a series of rules, called rungs, which can be executed sequentially during a PLC's cycle. The concept of rung can be seen as the basic building blocks of the ladder diagrams, so most of the literature on translating ladder diagrams to model checking models is centered around translating rungs.

There may be elements in each rung which are executed from left to right in a sequential way. This way, the output of each element in a rung becomes an input to another element. There may exist two important entities in each rung of a ladder diagram called coils and contacts. Coils are always to the rightmost side and act as a boolean variable output. On the other hand, contacts represent boolean input variables which may be either open or closed (negated). Connecting the elements in a rung in a serial way forms a logical conjunction while connecting in parallel forms a logical disjunction. Moreover, function blocks can be included in rungs for some PLC vendors programming tools as well.

For instance, the ladder diagram in Figure 4 contains only one coil labeled as f at the upper right side of the figure. The elements labeled a to e are contacts and each horizontal line containing contacts on them are rungs; there exists three rungs in the example which contains contact a-b, c-e and d respectively. Ladder diagrams can be interpreted as propositional logic formulae easily, which makes this kind of interpretation a frequently studied topic in model

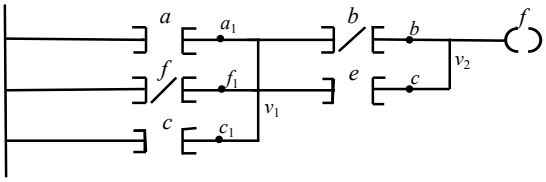

Fig. 4 An example Ladder Diagram snippet (James et al, 2014)

checking PLC software. An example program along with Ladder Diagrams can be seen in Figure 4. This piece of LD corresponds to the propositional logic formula $((a \vee \neg f \vee c) \wedge (\neg b \vee e)) \leftrightarrow f$

3.3 Modeling Languages

3.3.1 Sequential Function Charts

Sequential function charts are defined as elements structuring the internal organization of PLC programs and function blocks. Most of the time, each block in an SFC contains a ladder diagram pointing to a lower level abstraction in the PLC program. Not only SFC's are used to provide a broader view of the program with their structure similar to flowchart diagrams but also they can introduce parallelization by being able to represent multiple program flows within a single diagram. Moreover SFCs were inspired by Petri nets and an older Grafcet standard, so that it would be more appropriate to categorize SFC based studies separately from programming language studies, but rather as modeling studies with Petri nets.

SFCs bring structure to the elements inside a PLC program by defining steps, linked with action blocks and transitions. Program flow is actually composed of a series of special "step transitions" where by each transition the emerging step of the transition is deactivated and the next step is activated. An example to those steps and transitions of a Sequential Function Chart can be seen in Figure 5. Steps can be linked with an action block, which performs a control action when a step is activated. Each step in this execution can be modeled as one of the standard programming languages defined above or as an SFC model recursively. SFC program explicitly represents the execution order of program component units, which can be arranged in an alternating and/or parallel way.

3.3.2 Petri Nets

One of the most commonly used formal modeling approaches in describing PLC programs is using Petri nets (Peterson, 1981). A Petri net consists of places, transitions and arcs where each place may hold a number of tokens. Tokens are used to bring concurrency in Petri net execution, where a number

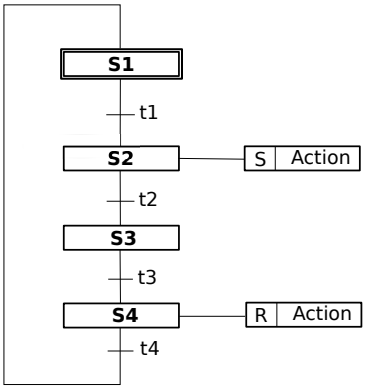

Fig. 5 Steps and Functions in a Sequential Function Chart Method (Fujino et al, 2000)

of tokens can be transiting among places in a Petri net. Transmission of a token from one place to another is constrained by the transitions and arcs connecting places to each other. Two or more places can be connected to each other over one transaction and multiple arcs. In order to connect two places, there should be an arc from one of the places to a transition and another arc from that transition to the other place. An example program modeled with a Petri net can be seen in Figure 6.

The tokens (indicated with black dots) inside places (indicated with 'P' labels) are the basic elements used to model parallel executions by floating over the transitions(indicated with 'T' labels) between the places. For the initial configuration, an arbitrary number of tokens can be present in the Petri Net. Tokens can perform place transitions only if there exists a transition between two places. There may be multiple tokens inside a place at a time. During petri net run, tokens perform transitions between the places at each step following the transition rules, which drive the parallel behavior of tokens. For example, if there exists a transition from a single place to a multiple number of places, the token is duplicated for each destination place. Conversely, if a transition connects many(assume n) places to a single destination place, there should be at least one token in each source place that is going to be merged with others in the destination place after the transition occurs.

Petri nets are frequently used in PLC program modeling and model checking purposes since they can be converted to PLC programs relatively easier than most of the other formal modeling approaches. Moreover, Petri nets are also frequently used in model checking purposes having a strong tool and analyzer support in the field. During modeling PLC programs many Petri net variants like Signal Interpreted Petri Nets and Colored Petri Nets (Jensen, 1987) are used.

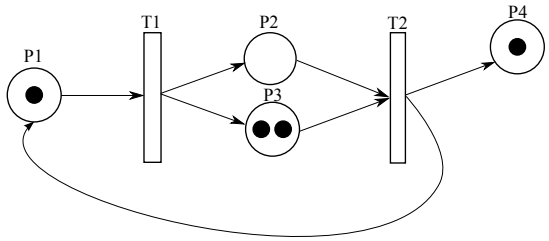

Fig. 6 An example Petri Net Model

3.4 Other Approaches

Studies on model checking PLC programs are not limited to the standard and conventional techniques described above but also a large number of studies exist using different kinds of programming languages and modeling approaches. Below, we give a brief description for each of the concepts used during our analysis in Section 8.

- PLC-Automata: A special extension of automata having formal temporal semantics defined with duration calculus. PLC-Automata (Dierks, 1997) can be transformed directly to PLC executable code.
- Timed Automata: Timed Automata (Alur and Dill, 1994) is originally a formal modeling methodology that is frequently used in model checking purposes. Instead of transforming the PLC Software model to a model checking formalism, directly modeling the system using Timed Automata is preferred in a few studies.
- Condition Event Systems: Condition Event System (Sreenivas and Krogh, 1991) is a discrete state formalism developed for modeling discrete event systems. It inherits functionality from Petri nets and can be directly model checked. Temporal variants of this approach is also used in some studies.
- Unified Modeling Languages: Unified Modeling Language (Rumbaugh et al, 2004), originally developed to model object oriented software intensive systems, is later extended to statechart models. This modeling approach is frequently used in modeling PLC software, and it has been used for model checking purpose as well in a couple of studies.
- MATLAB Statecharts: Different adoptions of statecharts (Harel, 1987) are present today, UML statecharts and Matlab statecharts being widely used two adoptions. Matlab statecharts are used in conjunction with Simulink Design Verifier for PLC program verification.

In addition to those approaches directly applied in relation with PLC program verification purposes, there also exist a number of studies where researchers use their own PLC modeling approach or their own model checker tools in order to contribute to the challenges faced by the practitioners of the approaches listed above. Some of them combined different techniques listed above to gain advantage from strengths of each approach. There also exist

some studies (de Assis Barbosa et al, 2007) (de Vasconcelos Oliveira et al, 2010) (Heimdahl et al, 2004) where the approach is not directly related to PLC model checking, but the process or the outcome can be used in such purposes therefore we chose to mention them as well at the end of Section 8.

4 Research Methodology and Classification of Practices

4.1 Previous Surveys

Before examining in detail the model checking studies performed on PLC program verification, we would like to explain the research methodology we have followed for the research and review process of the papers we have included in the survey. We have started the research process with a few studies that perform a similar survey in the past about verification of PLC programs or alike.

In the study by Frey and Litz, verification and validation activities on PLC programming is discussed over a generic control design process model proposed by the authors (Frey and Litz, 2000). In their study, they analyzed the integration process of formal methods in PLC programming and discussed various practices in different stages of this iteration process. Later they classified the verification approaches, formalisms used and methods applied during the integration process. Model checking was one of the methods in this classification among theorem proving, reachability analysis and simulation.

Later, the dissertation by Ralf Huuck contains a survey of model checking studies applied on PLC programs (Huuck, 2003). His study focuses on developing formal approaches on PLC programs specified in IL and SFC and proposes a model checking approach based on translating SFCs to CadanceSMV models. In his study, Huuck also provided a discussion of model checking approaches for PLC programming. In his discussion, it can be seen that most of the studies in the area are performed over IL models and a few studies exist on other programming approaches at the time.

Finally, the study by Younis and Frey provides a classification scheme for the works done in formalization of existing PLC programs (Younis and Frey, 2003). They classified the studies based on four criteria: sources used for the formalization, level of formalization, aim of formalization and the formal model used to describe the PLC program. Although their discussion mostly include model checker formalisms as the targets of PLC program translation, they also mention a few approaches on static analysis and reverse engineering as well. Our study can be seen as updating and expanding their study.

The latest survey presented above is dated back to 2003; during the last decade, practices on model checking has evolved in a noticeable manner especially in the area of FBD translation. Earlier studies focus on verifying textual PLC programs or ladder diagrams where only boolean variables are used. Beginning from 2000s FBDs started to take over due to their more modular

structure, ability to handle complicated programs more easily and availability of different types of variables.

Additionally, model checking tools are being continuously improved as well, most of the model checking tools have improved their efficiency and published new releases of their software. Moreover, the computing capabilities of hardware is also continuously increasing so it became possible to model check many complicated systems, which were not suitable for model checking before. An obvious example is the increase in studies aiming towards verification of real time properties. Three quarters of the number of timed automata based verification studies included in our surveys are performed after 2003.

Handling larger programs is another improvement that can be seen in latest studies. Even though the system sizes were being measured in terms of variables instead of function blocks in earlier days, latest studies report an improvement of a hundred times in larger sized systems. Comparisons in latter parts of our study show that FBD based verification studies are now able to handle thousands of variables where the numbers were less than a hundred for the studies performed using ladder diagrams.

4.2 Research Methodology

During our research process, we have used the surveys reviewed above as basis together with some very early studies published on the subject like the paper by Halbwachs et al. (Halbwachs et al, 1992) and Moon et al. (Moon, 1994). We have built our initial paper base by including all the papers reviewed by the surveys above and the early studies mentioned. We have applied a number of iterations by following the steps below until we were sure that the paper base is not expanding anymore.

1. Widely known electronic library resources(ACM Digital Library, Elsevier Science Direct, IEEE Explore, Springer Link and Wiley Online Library) are searched for the related papers cited by the papers in our paper base.
2. Widely known academic indexing sites (Citeseer, DBLP, Google Scholar, Microsoft Academic Search) are searched for the papers that cite the papers in our paper base.
3. Full range of academic studies of the authors that are present in our paper base are skimmed.
4. Mostly used keywords in our paper base (PLC, Model Checking, LTL, FBD, etc.) are searched in electronic library resources.
5. International Federation of Automatic Control's events and publications are directly searched.

After each iteration of the steps above, we applied a preliminary review and included the appropriate papers to our paper base. We keep track of both included and excluded papers to our paper base in order to rapidly eliminate any sort of duplicate reviews. At the end of our iterations, we have used the following criteria to be included in the detailed review process:

- Studies that use a present model checking tool in verification of PLC software like SMV, UPPAAL, etc.
- Studies that the authors have developed their own model checkers in verification of PLC software
- Studies that apply model checking on the PLC software developed by the programming languages included in the IEC 61131 standard.
- Studies that use modeling languages (Petri Nets, UML, etc.) in representing PLC software.

Following criteria is used to exclude papers from the paper base:

- Studies that use formal methods other than model checking like theorem proving.
- Studies that focus on test case generation, state reduction and specification representation even though we mention and cite them whenever needed.

At the end of our review process, we have reviewed 78 papers where 54 of the papers were included in the proceedings of related symposia, conferences and workshops; 16 of the papers were published in journals and the rest of the papers were technical reports, MSc/PhD thesis and books. Interestingly, all of the journal articles included in our survey has been published in a separate journal. A more coarse grained clustering can be done by the publishers of the journals where IEEE journals has the lead by 5 different journals. Even though the conference proceeding papers are more concentrated than journals, there are still 34 distinct conferences for the papers covered in our study. IEEE conferences covers a total of 31 papers published in the area; among those IEEE Conference on Emerging Technologies and Factory Automation proceedings contains 6 of the covered papers, followed by IEEE International Conference on Systems, Man, and Cybernetics contains 5 of the covered papers. Another notable clustering is in IFAC conferences, where 4 different conference proceedings contain 5 papers covered in this survey.

4.3 Classification of Practices

In this section, we present our main classification discussion on the studies that we are going to examine in more detail. Before presenting our main classification, we would like to mention the main model checking approaches and tools used in the studies that will be discussed. Briefly three main set of tools used in a wide range of studies, which are:

- SMV based tools, which include NuSMV (Cimatti et al, 1999) and CadenceSMV (McMillan, 1999). Symbolic model checking techniques and binary decision diagrams (McMillan, 1993) are applied in SMV based tools. Those tools can verify properties written in both Linear Temporal Logic(LTL) and Computation Tree Logic(CTL).
- Timed Automata based tools, which is mostly from UPPAAL family (Larsen et al, 1997) or Kronos (Yovine, 1997) in a few studies. Timed Automata is

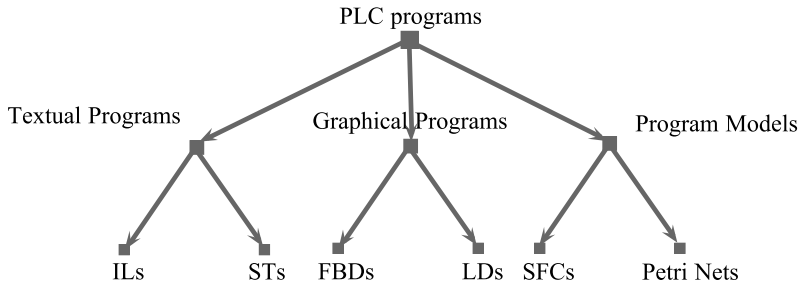

Fig. 7 Main classification of PLC programs used in classifications

an extension of automata with a set of real valued clocks. These clocks are actually positive integers that increase monotonically and in a synchronous way during automata run. Timed Automata based tools are used to perform model checking on real time system models and allow specifications in Timed CTL.

– SPIN model checker. SPIN is one of the major model checkers where the program models are expressed in Promela language and converted by SPIN to programs in C language to verify properties written in linear temporal logic.

Apart from those model checkers there are also studies performed using model checker Tina (Berthomieu et al, 2004) or authors' own model checker implementations.

Our main classification approach is examining the studies by the PLC programming or modeling language being used as the source for translation to the model checkers modeling formalism. As explained in the former section we have used a similar taxonomy presented in the IEC 61131 standard with the only exception of widely used Petri Nets examined in addition to SFC based models. A diagrammatic representation of the taxonomy we use in our classification is presented in Figure 7.

Second criterion in our main classification is the target model checking formalism and specific model checking tool used. In Tables 1 and 2 we present a matrix of all the studies we have examined, grouped in rows of the matrix according to their PLC programming/modeling approaches and grouped in columns of the matrix according to the kind of model checking formalism they use.

In Table 1 examined studies are classified according to the programming language and the model checking tool used in the study. It can be seen that the mainstream model checking tool used in the studies is SMV followed by UPPAAL. The main difference between these tools are the real-time model checking capability offered by UPPAAL where real time clocks can be included in the model. On the other hand SMV allows model checking timed properties implicitly. In SMV, temporal properties can be expressed (using temporal logics) by referring to an implicit "current time" and the properties

	Timed Auto.	SMV			SPIN[S]
	UPPAAL and Kronos[K]	SMV	NuSMV	CadenceSMV	Tina[T] and Others
Textual Programs	Willems1999 Zhou2009		Gourcuff2006 Pavlovic2007	Canet2000	Mader2001[S] Schlich2009 Biallas2012 Barbosa2012
Function Block Diagrams	Silva2008 Soliman2011 Enoiu2013		Pavlovic2010 Pakonen2013	Jeon2007 Yoo2008 Jee2010	Barbosa2012
Ladder Diagrams	Zoubek2003 Sarmento2008 Mokadem2010	Turk1997 Probst1997 Smet2002		Rossi2000	Moon1994 Bender2008 [T] Farines2011 [T] Barbosa2012
Sequential Function Charts	L'Her1999 [K] Bauer2004	Bornot2000 Fujino2000 Couffin2000		Bauer2001 Huuck2003 Bauer2004	Brinksma2000 [S] Mader2001 [S] Barbosa2012
Petri nets		Mertke2001	Frey2006 Grobelna2012 Grobelna2011	Weng2001 Klein2002 Gergely2010	Frey1998

Table 1 A General Classification of studies performed in Model Checking PLC Programs

are specified relying on the ordering of events with respect to the current time. The studies that contain model checking real-time properties using UPPAAL include heavier discussion of abstraction and state space reduction compared to SMV based studies.

In two of the timed automata studies Kronos is used (indicated with 'K' superscript) rather than UPPAAL. However both of these studies are rather outdated, which can be interpreted as UPPAAL dominating the timed model checking studies in PLC model checking. For SMV, a more balanced distribution of choices are present between NuSMV and Cadence SMV both in terms of numbers and recentness. There are also earlier studies using earlier versions of SMV model checker based on binary decision diagrams.

Apart from these two mainstream model checkers there are also studies, which use Promela/SPIN, Tina and other model checking tools, mostly authors' own implementations. In Table 1, studies that use SPIN are indicated with an 'S' superscript and studies that use Tina are indicated with 'T' superscript. Most of the SPIN based studies are performed around year 2000 where the two Tina based studies are relatively more recent compared to SPIN based studies.

An interesting comment on Table 1 can be the excessive use of FBDs in recent studies. All of the studies that use FBDs are performed after 2007 and a great portion of these studies are performed after 2010. On the other hand sequential function charts were mostly used between 2000-2005, they seem to be not preferred for more recent model checking studies. Another interesting point is the lack of timed automata studies using Petri nets. The capability of modeling timed properties using Petri nets explicitly can be the reason for the lack of such translations, the authors choose to either use Petri nets or timed automata when real-time modeling is needed.

	Timed Automata	SMV	Others
PLC-Automata	Olderog1999 Dierks2004		
Timed Automata	Witsch2006 Wang2007 Lahtinen2008		
Condition / Event Systems		Rausch1998	Hanisch1997 Kowalewski1999 Vyatkin2003
State Machines	Sacha2008	Klotz2009	
CFCs	Wardana2009		
Simulink and Data/State Flow Charts			Jimenez-Fraustro2001 Mazzolini2010
Other	Vulgarakis2009 (REMES)	Halbwachs1992 (LUSTRE) Thapa2006 (tMPSG)	Weissmann2011[S] (VKRC)

Table 2 Classification of studies performed using non-standard tools or languages

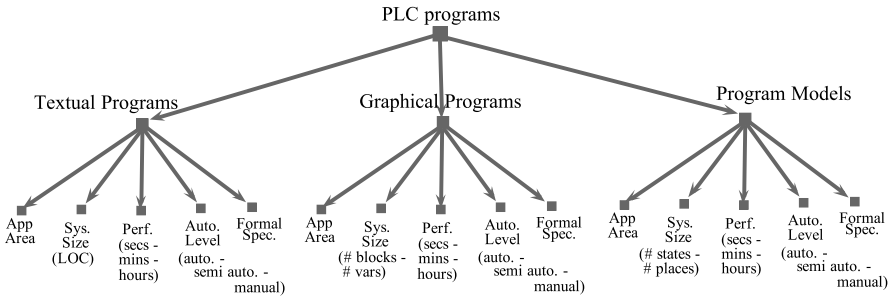

Fig. 8 Properties used in classification of PLC program verification studies

In Table 2 we present a similar classification for the studies that do not use IEC 61131-3 standard programming languages or Petri nets. A considerable amount of studies exist that use a modeling language derived from finite state automata such as PLC-Automata and Timed Automata. Other approaches include data and state flow charts and event systems where more recent studies are focused. Simulink is used in a couple of studies to perform verification using the built-in verifier. Timed automata is used more than SMV when non-standard languages are considered, because most of the time used modeling language is automata or state-transition based making it easier to transform into timed automata models.

Both these tables are presented to give a brief overview of the relation between the model checkers and the programming languages used in model checking PLC systems. In the following sections, we elaborate our overview by discussing the mentioned approaches above and making comparisons when possible.

In our classifications we use five main properties of performed studies explained below to make a clear distinction among the individual studies. A graphical representation of the classified properties is also presented in Figure 8.

1. Application area: The usage area of the PLC system where the model checking is performed upon is identified with this class. It can be interesting to check if any relations exist between certain usage areas and specific tools/techniques like the classic example of railway crossings and timed automata.
2. System Size: The unit used in system size can change according to the PLC programming language in the study. For instance, for textual programs the system size can be defined as the lines of program while for FBDs it can be the number of function blocks in the system model. Some studies prefer to provide the size of the state space during the model checking process however this number can be subjective, because of the modeling tool and state space reductions used.
3. Performance: The time spend during model checking process. We prefer to use a broad unit of measure for performance since the performance can change according to the system size and hardware used in model checking. We simply use 'seconds', 'minutes' or 'hours' to indicate an approximate duration.
4. Automation Level: We separate the studies that perform fully automatic process in converting the PLC program models to model checker's models. We present three classes of automation 'automatic', 'manual' and 'semi-automatic' where in semi-automatic conversions additional interventions are performed over automatic conversions either to perform abstraction of small modifications.
5. Formal Specification: Specification of the properties to be verified using a temporal specification language (LTL, CTL, TCTL, etc.) are also performed in an automatic way in some of the examined studies. We make a distinction by providing 'automatic', 'manual' and 'semi-automatic' classes.

We have also included an additional comparison about the kind of properties that has been verified in the studies. Although the properties that were checked can be intuitively guessed from the type of model checking tool used in each study, some studies do not fully utilize the capabilities of the tools they use. A typical example is to use timed automata in modeling the system and not to include any timed properties in the specifications that are checked. Our comparison tables contain the following 3 type of data.

1. Real time properties: This column is used to indicate if any timed properties have been verified in the study.
2. Correctness properties: The property to be verified can either be an invariant that is used to verify regular correctness properties (indicated with capital I) or the property can be a safety property ensuring that an unwanted situation never happens(indicated with capital S) or it can be a

liveness property ensuring the continuous execution of the system (indicated with capital L).
3. Specification logic: This column contains the temporal logic used in specification.

It should be noted that the properties above are indicated in the classification based on explicit examples in the paper instead of author claims.

5 Model Checking Textual PLC Programs

Textual PLC programs are the means of PLC programming practices where we exhibit the earliest studies in formalization for model checking. This is quite natural, because text based programs were being used earlier than FBDs and parsing them is more straightforward then ladder diagrams. One of the most prominent challenges in model checking textual PLC programs is reflecting timer on-delay instruction(TON) type of timers used in PLC programs for the purpose of ensuring the real-time properties. Basically, TON instructions are used to present a delay mechanism for their input signals. A TON's *true* input is reflected to its output only if the input signal is stable for a constant amount of time specified by the PLC programmer.

Also being one of the earlier studies in the area Mader et al. study on transforming IL programs to Timed Automata models (Mader and Wupper, 1999). They discussed the problem of TON timers and proposed two solutions: the first solution is using IL to program TON blocks and the counterpart is using automata to model TONs in the program. They indicated that it is more preferable to adopt the second approach since it is more modular and simpler. However in the future work by Mader et al. they have chosen to use Promela models instead of timed automata when performing model checking on an industrial case study (Mader et al, 2001). Interestingly this study is also one of the few studies where SPIN is used in PLC program verification rather than SMV or UPPAAL.

Almost during the same years Willems study a similar TON problem and came up with a similar solution where he used timed automata to model TONs in the system (Willems, 1999). Moreover he has dealt with zenoness issues that may arise and proposed solutions for such problems. Willems was able to reduce the state space size between 5 fold to 30 fold in his studies using Caesar/Aldebaran Development Package for performing state reduction on the produced models.

One of the latest studies that deal with the TON problem by using Timed Automata as well is by Zhou et al. (Zhou et al, 2009) where the authors claim they have expanded Willem's work. In their study Zhou et al. used four different modules namely "Coordinator" to model PLC synchronization, "Program" for PLC program, "Environment" for I/O and "Interruption" to model time based interruptions. Even though the first three modules are conventionally present in most of the studies in this area, interruption module is specific to this study.

	App. Area	Syst. Size	Performance	Auto. Level	Formal Spec.
Willems1999	N/A	18 Lines	N/A	Automatic	N/A
Canet2000	Tool Changing	89 Lines	N/A	Automatic	Manual
Mader2001	Batch Plant	N/A	Minutes	Manual	Manual
Gourcuff2006	N/A	4000 vars	Seconds	Automatic	N/A
Pavlovic2007	Counter	N/A	Min.-Hours	Semi-Auto.	Manual
Schlich2009	Counter	N/A	Seconds	Automatic	Manual
Zhou2009	N/A	N/A	N/A	Automatic	Manual

Table 3 A classification of studies performed with Textual PLC Programs

Timed Automata is not the only formalism used in IL model checking. There are two studies, which utilize SMV models in order to model check IL programs as well. The earlier study by Canet et al. deals with single smaller modules and does not consider the timers during their studies (Canet et al, 2000). On the other hand Pavlovic et al. include interesting discussions in their study where they provide a meta description of the IL language to their translation process to be able to adapt the possible modifications in IL standard in the future (Pavlovic et al, 2007). Their discussion also references a method by Peleska and Haxthausen (Peleska and Haxthausen, 2007) to check the behavioral equivalence of their formal models with the original PLC program. They also use SMV as the model checking formalism.

Another important commonality in textual program transformation studies is the dominant usage of IL over ST. Most of the papers below use mainly IL and some of them use ST programs secondarily in the transformation process. Gourcuff et al. use ST and perform dependency analysis between the variables in the program before transforming the program to SMV models (Gourcuff et al, 2006). They have also compared their results with DeSmet et al.'s study (Smet and Rossi, 2002) where the results show significant improvement.

Lastly we would like to mention Schlich et al.'s study where IL programs are model checked directly without using any conventional formalism (Schlich et al, 2009). They have used "concrete" and "abstract" simulators to generate state spaces from IL programs where concrete simulators generate state(s) for each PLC cycle. On the other hand abstract simulators aggregate suitable states to reduce the state space. Their results show that the same example in Pavlovic et al.'s study (Pavlovic et al, 2007) can be checked in 6 seconds where in Pavlovic's work the process was taking 8 hours. They also compare their work with another study by Huuck (Huuck et al, 2003) and show significant improvements as well.

Examining Table 3 and Table 4[1] we see that the studies that explicitly state the size of the system(in terms of number of lines) do not consider the performance of the model checker. Conversely the system size is not mentioned for the studies that mention the system performance. Nevertheless, it can be inferred from the results that model checking is performed in acceptable times for most of the studies. Model checking a 90 line program may not seem large enough for realistic systems, however undersized experiments are unavoidably

[1] Papers that do not include explicit information were omitted

		Correctness			
	Real time	Invariance	Safety	Liveness	Spec.Logic
Canet2000	No	Yes	Yes	Yes	LTL
Mader2001	No	Yes	No	No	LTL
Schlich2009	No	Yes	No	No	CTL
Zhou2009	Yes	Yes	No	No	CTL

Table 4 Properties checked when model checking textual PLC programs

common for the model checking case. An automatic translation between PLC program and model checker's input language is performed most of the time due to the ease of parsing textual programs. On the other hand none of the studies mention automatic generation of specifications to be checked compared to a few studies present for other programming models. Even though the reason behind this situation can be the low level nature of textual representations that doesn't contain any abstractions, automatic specification extraction area seems to be an open area for this field of study.

Among all the studies discussed above Willems et al.'s study and Zhou et al.'s study are the only ones that used timed models in model checking process distinguishing them form other studies. These studies can handle simpler programs compared to the more recent studies by Pavlovic et. al's and Schlih et al.'s studies being able to handle much larger state spaces. Lastly, we would like to mention Mader et al.'s study including very detailed examples on a practical case study.

6 Model Checking Graphical PLC Programs

6.1 FBD Programs

The most recent studies on model checking PLC programs are performed on FBD programs; almost all of the studies examined below belong to the last five years, which point to FBDs being the most recently used means of PLC program verification in this context. When it comes to model checking formalisms studies almost split in half in using either SMV or UPPAAL models.

The work of Jee et al., Jeon et al. and Yoo et al. all focus on model checking a PLC program of a nuclear power plant control system by using Verilog models and CadenceSMV for the model checking process. Again common to all studies a rule based engine is used in performing translations. Jeon et al.'s and Jee et al.'s study specifically focus on producing more understandable counterexamples (Jeon, 2007) (Jee et al, 2010) since the output of their tool produce tables of values for all the variables in the system. To provide a consistent translations from FBDs to model checker's language both studies required assumptions on FBD programs like predefined execution orders and type safety. On the other hand Yoo et al. use VIS verification technique (Brayton et al, 1996) to check the conformance of behaviors between their FBDs and Verilog models (Yoo et al, 2008).

Pavlovic et al. use their own intermediate format, which they call *tFBD* after they transform their FBD program into a text based representation they call *textFBD* (Pavlovic and Ehrich, 2010). By defining operational semantics of *textFBD* format isomorphic to FBD semantics they assure the equivalency between models in their translation process. They claim that their tFBD format, which is based on compacting *textFBD* to propositional logic formulae, dramatically reduce the state space during the model checking process realized with SMV. The compaction process combines chains of assignments(which is frequently present in FBDs) into single assignments reducing the amount of variables(especially temporary variables) used in *tFBD*'s logic formulae. They apply their method in the area of railway automation to a small and a more general case study and report that the state space is reduced in a dramatic way from 10^{65} states to 10^{14} states for one of their examples.

Pakonen et al. also work on translating FBD programs to SMV models for verification purposes; their work is focused on generating an Eclipse based tool, which does not perform automatic transformations but provide vendor independence (Pakonen et al, 2013).

One of the studies which use UPPAAL and Timed Automata for model checking is the work by Soliman et al. where a rule based transformation engine is used to transform safety function blocks, connections, inputs and triggers in an FBD separately into Timed Automata models (Soliman and Frey, 2011). Unfortunately their paper does not contain a detailed evaluation on the effectiveness of their work.

Two studies we have included in this comparison focus on generating test suites using the model checking tool UPPAAL to be used in PLC testing. Even though authors do not directly apply model checking, their approach can influence researchers and practitioners working in model checking PLC programs. The first study in this particular area is performed by Enoiu et al. (Enoiu et al, 2013b) (Enoiu et al, 2013a) where they were able to generate 40-50 state test suites in less than a second from 30 FBD PLC programs. Another study by Silva et al. also focuses on test generation from standard FBD programs (da Silva et al, 2008) by generating a synchronization automaton to represent PLC cycles and a behavior automaton for each FBD.

Table 5 and Table 6[2] summarizes the important aspects about the model checking studies on FBD programs. Translation from FBD to model checker language is done automatically for most of the cases. Verification of systems up to the level of thousand blocks was possible even though the time required for verifications is not explicitly included in most of the studies.

6.2 LD Programs

A wide range of studies exist for model checking LD programs spanning over SMV and UPPAAL models as well as Tina model checker. LD program based

[2] Papers that do not include explicit information were omitted

	App. Area	**Syst. Size**	**Performance**	**Auto. Level**	**Formal Spec.**
Jeon2007	Nuclear Plant	16 blocks 7 vars	N/A	Semi-Auto.	N/A
Silva2008	Hydrogen Gen. Unit	19 blocks 12 vars	N/A	Automatic	N/A
Yoo2008	Nuclear Plant	1500 blocks 1000 vars	N/A	Automatic	Manual
Pavlovic2010	Railway Interlock	100 vars	minutes	Automatic	Manual
Soliman2011	Safety App.	6 blocks	N/A	Automatic	N/A
Enoiou2013	Train Control	30 blocks	$<$ 1 sec.	Automatic	Automatic
Jee2010	Nuclear Plant	20000 blocks 9000 vars	N/A	Automatic	N/A
Pakonen2013	N/A	N/A	N/A	Manual	Manual

Table 5 A classification of studies performed with FBDs

		Correctness			
	Real time	Invariance	Safety	Liveness	Spec.Logic
Pavlovic2010	No	No	Yes	No	CTL
Enoiu2013	No	Yes	Yes	No	CTL
Jee2010	No	Yes	Yes	No	N/A

Table 6 Properties checked when model checking FBD based PLC programs

studies span over time as well, there exists very early studies that utilize LDs as well as recent studies. For the case of LD model checking the most recent studies generally use UPPAAL where earlier studies chose to use SMV variants to perform model checking.

Very early studies by Turk et al. and Probst et al. both use NuSMV as model checker and also they both use relay logic ladders, the early versions of ladder diagrams. Turk et al. discussed the main challenge as transforming to the implicit time domain present in SMV (Turk et al, 1997) where Probst et al. handle the issue by modeling the hardware and non-deterministic human behavior separately to produce more realistic inputs during model checking process (Probst et al, 1997).

A more recent study by DeSmet et al. uses a Python based parser to transform each rung in LDs to a separate SMV model while the main challenge is to conserve the connections between the rungs among SMV models (Smet and Rossi, 2002). Even though the details of the transformation process are not provided, a considerable amount of discussion is provided on specifying temporal properties of the system. By using their system they were able to model check three different systems having between 27K and 16M states during model checking. The model checking process is performed between 1 seconds and 4 and a half hours respectively.

Rossi et al. have used CadenceSMV as a tool and translated text representation of LDs using a 6 ruled transformation engine (Rossi and Schnoebelen, 2000). Although the paper does not contain a clear evaluation of the approach they focus on TON semantics and how they can be handled in a large context.

Zoubek et al. also focused on TONs in their paper, but they chose Timed Automata and UPPAAL for model checking (Zoubek et al, 2003). Conven-

tionally they model the user input, the program behavior and the PLC cycle separately, but their transformation works on a total of seven different instructions. An important contribution of their work is to use program slicing in reducing the state space of the produced system. They also provide additional manual abstractions to further shrink the state space. As a result of their studies they were able to reduce the model checking duration of their case study to a few minutes, which normally took unmanageable amount of time.

UPPAAL is also used by Sarmento et al. in their studies, but the models do not include explicit time properties (Sarmento et al, 2008). They use a finite state intermediate model, which contains integer and boolean variable annotated transitions. They provide a seven step modeling procedure for their methodology however their discussions do not include any aspect about automation of their process. Recently in Mokadem et al.'s study on multitasking PLCs are model checked using Mader-Wupper model (Mader and Wupper, 1999) with further manual modifications as an intermediate model to effectively handle TON timers and reduce state space (Mokadem et al, 2010).

Specific to LD model checking, two studies have used Tina as model checker. In Bender et al.'s study (Bender et al, 2008) a model driven approach is applied by using ATL (Jouault and Kurtev, 2006) transformations over LDs to produce timed Petri nets, which then can be automatically transformed to Tina models. A rule based translation is used in LD translation and race conditions are handled by checking if the stabilizing inputs yield to stable outputs. The stability of the output variables are checked by using two timed petri net places for each variable's true and false state respectively. Absence of race conditions are checked by observing stabilized outputs as a result of stabilized inputs. Authors claim they were able to reduce the state space of a six actuator seven sensor system from 7 million states to 40 states using Tina. A later study with Tina is carried out by Farines et al. where a model driven engineering approach is used in transformation of LDs to an intermediate form of FIACRE platform (Farines et al, 2011) (a timed transition system in particular). Their work is very similar to Bender et al.'s work except the intermediate format they use.

Lastly it is worth to mention James et al.'s study where LDs are utilized to produce LTL formulas to be used in model checking (James et al, 2014). In most of the studies examined in this paper, such specifications are produced manually which makes this study more valuable.

Model checking LD programs is applicable on systems having less than 100 variables as the Table 7 depicts. For most of the studies the process was completed in an order of minutes while automatic translation is performed in around half of the studies. In the study by Bender et al. (Bender et al, 2008) performance was discussed over the size of the Petri net model, which is used as an intermediate format so it was considered likewise in the comparison table as well. In Table 8, we can see that most of the studies include explicit examples of the properties(especially safety properties) that were checked.

	App. Area	**Syst. Size**	**Performance**	**Auto. Level**	**Formal Spec.**
Probst1997	Screw Conveyor	74-93 vars	minutes	Semi-auto.	Manual
Turk1997	Chemical Plant	24-93 vars	minutes	Manual	Manual
Rossi2000	N/A	N/A	N/A	Automatic	Manual
DeSmet2002	Machining Line	30 vars	secs. - hours	Automatic	Manual
Zoubek2003	Pumping Line	39 vars	minutes	Semi-auto.	Manual
Bender2008	N/A	23-31 places	N/A	Automatic	Automatic
Sarmento2008	Gas Burning Equipment	N/A	N/A	Manual	Manual
Mokadem2010	Pinion Identifier	N/A	seconds	Manual	Manual
Farines2011	Pneumatic	N/A	seconds	Automatic	Manual

Table 7 A classification of studies performed with LDs

		Correctness			
	Real time	Invariance	Safety	Liveness	Spec.Logic
Probst1997	No	Yes	Yes	Yes	CTL
Turk1997	No	Yes	Yes	Yes	CTL
Rossi2000	No	Yes	Yes	Yes	CTL
DeSmet2002	No	Yes	Yes	Yes	CTL
Zoubek2003	Yes	Yes	Yes	No	TCTL
Bender2008	No	Yes	Yes	No	LTL
Sarmento2008	No	Yes	Yes	No	CTL
Mokadem2010	Yes	Yes	Yes	Yes	TCTL
Farines2011	No	No	Yes	No	CTL
James2014	No	Yes	Yes	No	Lustre

Table 8 Properties checked when model checking LD based PLC programs

Most of the time CTL is used as a specification language, a few studies verify timed properties and use TCTL.

7 Model Checking PLC Program Models

7.1 SFC Models

Active research on using SFC models for model checking purposes mostly fall between 2000 and 2005. Even though SMV models have been the primary focus in SFC translation studies, there also exists work using timed automata in the process.

An early work by L'Her et al. uses Kronos tool for model checking process by inferring temporal properties of SFC diagrams (L'Her et al, 1999). In their paper authors examine the corresponding elements in timed automata models for sets of activities that can be present in SFC diagrams. They apply their approach on an 8 state SFC, but the resulting model could not be checked by Kronos since it includes 250K transitions, way too much for Kronos to check. They were able to reduce the state space to around 100 transitions by

adding constraints on the translation process and by eliminating unnecessary variables in SFC states.

Lamperiere-Couffin et al. have performed translations to SMV models by expressing the behavior in SFC steps using propositional logic formulae (Couffin and Lesage, 2000). These formulae are later used in building state transition conditions of the automata in SMV models. The largest state space checked by the authors contains 10^6 states, taking 4 seconds to be model checked. Citing this work, a paper by DeSmet et al. also mentions SFC based model checking and summarizes the research group's many PLC model checking studies in their paper (Smet et al, 2000).

The study by Fujino et al. mainly performs simulations on Petri net models translated from SFC diagrams' (Fujino et al, 2000). They also claim they were able to easily convert Petri net models into SMV models and perform model checking, but did not include a detailed evaluation of this process. Many different techniques are used in combination by Brinksma et al., where they perform translation from SFC and IL initially to SPIN models and perform state reduction by selecting states belong to cost optimal schedules generated using UPPAAL CORA (Brinksma and Mader, 2000). Another study by Bornot et al. focuses on reachability properties of SFC steps and did not include output variables in their SMV models in this respect (Bornot et al, 2000).

CadanceSMV was commonly used in more recent studies on SFC model verification. Bauer et al., in two different studies have verified nuclear power plant control programs (Bauer and Huuck, 2001) (Bauer et al, 2004). In the earlier study they have used variables to represent actions while in the latter one they were able to use automata for this purpose. Their main challenge in the second study was eliminating malformed sequences in SFC sequences, which they perform by searching for predefined subgraphs in the graphs generated from SFC models. They were able to model check a model with 40 different automata in about 15 minutes.

Finally, Huuck et al. try to identify unsafe and unreachable states in SFC models (Huuck et al, 2003). They use model checking to search for some rules that violate safeness of the model, which can be done by reachability analysis in state space generated by model checking. They claim they obtain successful results even for large SFCs, but did not explicitly include how large the checked SFC were.

Table 9 compares the studies on SFC programs where model checking was feasible at around ten states. For two of the studies the model checking was evaluated using the number of states generated during the model checking process indicated with TS (Transition System) states. The level of automation is above average in SFC based studies as well, where most of the studies perform at least a semi automatic translation where abstractions are applied after the automated translation process. In Table 10, we can see that in model checking SFC based programs, generally CTL is used. An interesting fact is none of the studies on model checking SFC programs verify real-time properties although SFC models inherently involve parallelism.

	App. Area	**System Size**	**Performance**	**Auto. Level**	**Formal Spec.**
L'Her1999	Production Cell	7 SFC states	N/A	Semi-auto.	Semi-auto.
Bornot2000	N/A	8 SFC states	N/A	Automatic	Manual
Brinksma2000	Batch Plant	24 SFC states	seconds	Manual	N/A
Fujino2000	Cooling and Alarm	4-8 SFC states	N/A	Semi-auto.	Manual
Couffin2000	Manufacturing	10^6 TS states	seconds	Semi-auto.	Manual
Bauer2001	Chemical Plant	14 SFC states	seconds	Automatic	Manual
Huuck2003	N/A	N/A	seconds	Automatic	Manual
Bauer2004	Chemical Plant	14 SFC states	minutes	Automatic	Manual

Table 9 A classification of studies performed with SFCs

		Correctness			
	Real time	Invariance	Safety	Liveness	Spec.Logic
LHer1999	No	No	Yes	No	CTL
Brinksma2000	No	Yes	No	Yes	LTL
Bornot2000	No	Yes	Yes	Yes	CTL
DeSmet2000	No	Yes	Yes	Yes	LTL
Fujino2000	No	Yes	No	No	CTL
Lamperiere2000	No	Yes	No	No	CTL
Bauer2001	No	Yes	Yes	Yes	CTL
Huuck2003	No	Yes	Yes	No	CTL
Bauer2004	No	Yes	Yes	Yes	CTL

Table 10 Properties checked when model checking SFC based PLC programs

7.2 Petri Net Models

There exist a huge number of studies on model checking Petri nets in the literature not only focusing PLC program models but also embedded systems and many other areas where Petri nets are used. We will be focusing on the ones that explicitly mention the area of application as PLC program verification in our discussions.

Earlier studies also discuss how Petri nets can be used in PLC program modeling purposes. For instance in Frey et al.'s work the usage of Signal Interpreted Petri Nets (SIPN) in control systems and the usage of their verification tool Netmate, on a dissolving tank example (Frey and Litz, 1998) are demonstrated. In a later study of Frey on SIPNs, he utilizes hSIPN (hybrid SIPN) to be able to fold states of Petri nets and presents analysis on such models (Frey, 2003). Frey et al. apply model checking in a later short paper by presenting a multi-purpose PLC programming toolbox (Frey and Wagner, 2006). In SIPN toolbox the capability of exporting to NuSMV models is also present.

In this area Frey has also co-authored many other papers. In Mertke et al.'s work an extensive study of modeling PLC programs and the behavior of the environment is performed (Mertke and Frey, 2001). They have combined Petri net model of the PLC and the environment to perform a complete model checking practice. Moreover they also transform the timed requirements to be checked from a German semi-verbal presentation, which is not frequently performed for the studies in PLC model checking.

	App. Area	Syst. Size	Performance	Auto. Level	Formal Spec.
Frey1998	Dissolv. Tank	6 places	N/A	N/A	N/A
Weng2001	Air Chamber	5 places	N/A	N/A	Manual
Mertke2001	Air Chamber	5 places	N/A	Automatic	Automatic
Klein2002	Manufact.	55 places	N/A	Automatic	Manual
Frey2006	N/A	N/A	N/A	Automatic	Semi-auto.
Gergely2010	Mixing Tank	5 places	N/A	Manual	Manual
Grobelna2011	Fluid mixture	9 places	N/A	Manual	Manual
Grobelna2012	Drink prod.	20 places	N/A	Automatic	Manual

Table 11 A classification of studies performed with Petri nets

The work of Weng et al. contains formalization of Petri net places. Inputs and outputs to CadanceSMV models (Weng and Litz, 2001) is discussed on the control system of an air chamber. In their study Klein et al. adopt hSIPN approach (Frey, 2003) and perform CadanceSMV transformation with the approach in Weng's study on the verification of a manufacturing system (Klein et al, 2002). They also transform SIPN models to SFC models and re-model check to validate their approach.

Apart from Frey et al.'s work, an earlier study is performed by Heiner et al. where Petri nets are not used in directly modeling PLC programs but as an intermediate format to be generated from IL program (Heiner and Menzel, 1998). However their study only includes this translation process, model checking practice is left as a future work. On the contrary, a recent study by Gergely et al. performs translation to SMV models manually, but discusses the model checking process and focuses on specification of the properties with CTL (Gergely et al, 2010).

In a series of studies by Grobelna et al. Control Interpreted Petri nets are transformed to a rule based textual intermediate format called logical models and transformed to NuSMV models by a rule based translation engine (Grobelna and Adamski, 2011) (Grobelna, 2011) (Grobelna, 2012). Lastly, Nemeth et al. translate FBDs to Colored Petri nets to use them as intermediate formats in model checking a nuclear power plant's control system (Németh and Bartha, 2009).

Interestingly in none of the studies we have discussed a sound performance evaluation is present for Petri net based model checking as seen in Table 11. This situation drives us to assume that Petri nets with around 5 to 20 places can be model checked in applicable durations. A single study where a Petri net with around 50 states was model checked was performed by Klein et al. (Klein et al, 2002), however the authors state in their work that additional abstractions can be necessary when transforming from Petri nets to PLC models. These additional abstractions are applied by compacting repeated structures inside the Petri net into a single place. Table 12[3] contains similar results to the SFC property verification results, none of the studies explicitly include verification of real-time properties and most of them use CTL as specification logic.

[3] Papers that do not include explicit information were omitted

		Correctness			
	Real time	Invariance	Safety	Liveness	Spec.Logic
Mertke2001	No	Yes	Yes	Yes	CTL
Weng2001	No	Yes	Yes	No	CTL
Klein2002	No	Yes	Yes	No	LTL
Gergely2010	No	Yes	Yes	Yes	CTL
Grobelna2011	No	Yes	Yes	No	CTL
Grobelna2012	No	Yes	Yes	Yes	CTL

Table 12 Properties checked when model checking Petri Net PLC program models

8 Other Approaches That Use Model Checking

In spite of the large number of studies using IEC 61131 standards, PLC model checking is not limited to translation from standard PLC programming languages and modeling languages to a limited set of model checking tools. There also exist a large number of studies using a variety of different formats/tools to make the approach more effective and easy to apply for the community. Additionally, exploring the state space of PLC programs is not limited to model checking, it can also be used to generate a wide range of test cases, inspiring a number of academic research in the area.

PLC-Automata are a specific type of automata, which can define machines that periodically polls inputs and operate on them (Dierks, 2001). Formal semantics of PLC-Automata has been defined in duration calculus and such automata can be directly translated to PLC programs. Dierks et al. performed translation from PLC-Automata to timed automata models and validate their translation by verifying the same set of properties with duration calculus and translated timed automata (Dierks, 2004). They have used Kronos and UPPAAL for model checking and show that model checking is viable for tiny and small systems. Olderog et al. transformed constraint diagrams obtained from user specifications to PLC-automata and use PLC-Automata as an intermediate format (Olderog, 1999). Model checking PLC-Automata is performed by translating PLC-Automata models into timed automata models using Moby/-PLC, a tool developed by Dierks et al. (Dierks and Tapken, 1998).

There also exist some other studies that use directly modeling PLC and its environment using timed automata. For instance Wang et al. used UPPAAL to model check a controller (Wang et al, 2007) that control the motions of a theater steeve that lights, screen and curtains are adorned to. Witsch et al performed a similar study by modeling PLC based ethernet controllers directly using Timed Automata (Witsch et al, 2006). Another study is by Lahtinen where he checked an arc protection control system modeled in timed automata (Lahtinen, 2008). He presents a satisfying evaluation of the timed automata models and memory consumption/model checking time. Even though these studies' subjects are PLCs and they use model checking, they did not perform a full integration of formal methods to their verification process.

More than a few studies also exist where Condition/Event systems (C/E) are used in PLC program verification (Sreenivas and Krogh, 1991). In Hanisch

et al.'s study a variant of C/E's (Timed Net C/E[4]) are used and IL of PLCs are transformed to C/E models (Hanisch et al, 1997). They use their own model checking tool in their study. Another early study by Rausch et al. also uses Timed Net C/E and transform them to SMV models using a rule based engine (Rausch and Krogh, 1998). Kowalewski et al. also used C/E's together with the HyTech tool (Henzinger et al, 1995) to perform reachability analysis (Kowalewski et al, 1999). A more recent study by Vyatkin et al. also uses net C/E's and presents a framework supporting conversion from state charts and model checking using SESA tool (Vyatkin et al, 2003). Pang et al. performs conversion from function blocks to C/E's, but did not apply model checking in their studies (Pang and Vyatkin, 2008).

With the widespread usage of object oriented design and UML models there also exist some studies that use UML state charts in model checking process. Sacha et al. defined finite state time machines and use it as an intermediate format in conversion between state machine diagrams and UPPAAL models (Sacha, 2008). Klotz et al. also use UML state chart models and transform them to NuSMV models in verification of a case filling machine (Klotz et al, 2009). They were able to verify basic liveness and safety properties in around 80 seconds for a system model with three state charts.

Wardana et al. used Continuous Function Charts (CFC), a graphical programming language widely used in process industry, and model check a state space with three million states around 50 seconds using UPPAAL (Wardana et al, 2009). Mazzolini et al. used MATLAB state flow charts and perform verification of a shoe manufacturing plant model with Simulink Design Verifier in 35 seconds where the model contained 28 states 34 transitions and 21 variables (Mazzolini et al, 2010). Jimenez-Fraustro et al. also uses Simulink in verifying PLC programs (Jiménez-Fraustro and Rutten, 2001) modeled using a data-flow language SIGNAL (LeGuernic et al, 1991). Weissmann et al. chose to apply model checking approach on PLC programs of industrial robot systems programmed using a special purpose VKRC language. In their paper, they translate VKRC programs into Promela models and perform model checking using SPIN (Weißmann et al, 2011). They focused on deadlocks in their studies and were able to perform successful model checking to systems with around a thousand variables belonging to 10 different processes in around 2 minutes. The study by Anjos et al. (Anjos et al, 2013) can also be mentioned where LabView-UPPAAL conversion in order to model check robot controller systems. Even though a practical PLC program conversion wasn't implemented in the study, the authors mentioned the ease of conversion from LabView models to PLC programs in the paper.

In a few other studies non-conventional, or special design modeling languages have been used to specify PLC programs. Thapa et al. used timed version of their Message Based Part Graph (MPSG) modeling language and transformed PLC models to SMV models (Thapa et al, 2006). Vulgarakis et

[4] Timed Net C/E's actually use Petri nets in representation of internal dynamics. Nevertheless we will be discussing them together with other Condition Event System based approaches

al. use REMES, a modeling language for embedded systems and extend the language for interrupt support to be used in PLC model checking with UPPAAL (Vulgarakis and Causevic, 2009).

Biallas et al.'s implementation (Biallas et al, 2012), called Arcade.PLC, uses an internal representation that can be obtained by transforming text based formats: structured text and instruction list. Their system also supports Siemens SIMATIC S7's statement list format. They also implement their own model checker operating on their internal representation format and used abstract interpretation to implement the model checker. Their model checker is capable of model checking past time LTL and ∀CTL specifications.

In their work (Barbosa and Déharbe, 2012), Barbosa et al. supports a wide range of IEC61131-3 standard PLC programming languages(ST,SFC,FBD and LD) coded in PLCOpen[5] XML format by implementing adapters that transform program organization units to the B-method's (Leuschel and Butler, 2003) specification format. They used the ProB model checker (Abrial, 2005) to verify safety and liveness properties of the door subsystem of trains in a railway project in about ten minutes.

Since most of the widely used model checkers merely exist in very early days, earliest studies use their own tool for model checking like the study by Halbwachs et. al using LESAR verification tool (Halbwachs et al, 1992) and Moon et al. using relay ladder logic and their own model checker implementation (Moon, 1994).

As a final group of studies, we shall mention automatic test case generation and conformance testing using model checking tools and models on PLC systems. Studies by Barbosa et al. and Oliveira et al. use binary logic diagrams, a standard defined by instrument society of America, which is then transformed into IEC 61131-3 standards and test case generation is performed (de Assis Barbosa et al, 2007) (de Vasconcelos Oliveira et al, 2010). Both of the studies use UPPAAL TRON and focus on conformance of models and PLC programs. Different from these studies Heimdahl et al. used NuSMV to model check a flight guidance system modeled using $RSML^{-e}$ (Requirements Specification Model). During model checking process Heimdahl et al. provided model checker with test criterion formulations as a verification conditions. That way NuSMV creates a trace that can be used in testing purposes (Heimdahl et al, 2004).

All of the studies discussed above provide a different approach to solve the problems they face during model checking PLC programs using conventional approaches. Reimplementing the studies listed above can be challenging; however their way of solving the shortcomings of standards in their domains can be very influential for the researchers and practitioners working on the area.

[5] PLCOpen XML formats for IEC61131-3 standards: `http://www.plcopen.org/pages/tc6_xml/downloads/tc6\_xml\_v201\_technical_doc.pdf`

9 PLC Model Checking in Industry

Proper adoption of formal methods is an old debate subject in software industry rooted back to 1990s (Hall, 1990). In case of automation and control industry, the concerns for obtaining the necessary expertise doesn't vanish. In their paper on formal methods in PLC programming, Frey and Litz stated in 2000 "'*Although being a rather intuitive discipline for a long time, industrial PLC programming will be more and more supported by formal methods*"' (Frey and Litz, 2000). In this section, we would like to mention some applications in the industry that adopt the approaches and/or tools in the papers we have examined in the former sections.

The earliest attempts on using model checking on aviation industry was Nasa's Java PathFinder, where autonomy flight software was transformed to Promela models and checked by SPIN model checker (Havelund et al, 2000). These earlier attempts weren't able to gain wider usage in avionics industry until recently.

The article by Darren Cofer, Steven Miller et al. (Cofer et al, 2008) grounds four barriers in using formal methods in industry and especially in avionics industry. Three of these barriers are, the cost of using formal analysis, building consistent models with the problem and the use of unfamiliar notations. Cofer claims these barriers can be overcome by using model based development. In the paper, the fourth barrier which is performance requirements of tools is being improved as the Moore's law progresses.

In a study on model checking Airbus' ground spoiler(part of an aircraft wing flaps) controller function, Lustre specification language and Luster model checker were used by Bochot et al. (Bochot et al, 2009). The study contains a detailed discussion of the model checking the outcomes of the approach; the two key problems mentioned in those outcomes were the 48 hour verification time using a decent computer and the difficulties in transforming informal specifications to formal ones.

In 2009 Steven P. Miller commented about the same situation in his paper and claimed there is a growing application area for Model Checking by the utilization of Model-Based Development tools like Matlab Simulink®[6] and Esterel Technologies Scade Suite™[7] especially in avionics and automotive industries.

A recent study by Miller et al in 2010 (Miller et al, 2010) introduces the utilization of Halbwachs et al.'s approach (Halbwachs et al, 1992) in an adaptive airline control system. Rockwell Collins and University of Minnesota has collaborated to represent Simulink models and Stateflow charts in Lustre formal specification language as an intermediate format. From Lustre format, they were able to transform the specifications into the input language of three different model checkers including SMV and two different theorem provers(see

[6] The Mathworks, Simulink Product Description: `http://www.mathworks.com/help/simulink/gs/product-description.html`

[7] Esterel Technologies, SCADE Suite Product Description: `http://www.esterel-technologies.com/products/scade-suite/`

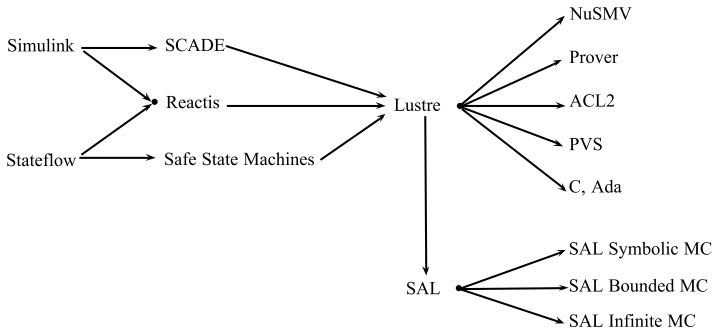

Fig. 9 Model Checking by Model Based Development as implemented in (Miller et al, 2010)

Figure 9). In this study, they were able to check around 500 properties and corrected around 100 errors this way.

The use of model checking PLC programs is not only limited to avionics industry, it has also been applied in railway control systems. A very recent study by Ferrari et al. works on General Electric Transportation System's Automatic Train Protection system by transforming Simulink programs to NuSMV models (Ferrari et al, 2013). There are also other studies (Faivre and Benoit, 1999) (Leuschel et al, 2011) in the same domain in industrial sized systems however their primary focus are not programmable logic controllers.

In addition to model checking, the application of formal methods in industrial systems is a very broad topic, which needs the inclusion of various different aspects of formal methods and also widely applied techniques like Discrete Event System Approach (Dacharry and Giambiasi, 2007) (Budha et al, 2008). Surveys that focus on industrial areas rather than PLC programs can also be found in the literature (Fantechi and Gnesi, 2011) (Lahtinen et al, 2012).

In this section we have tried to summarize recent advances in industry that transform PLC programs and utilize model checking directly on them. It can be seen that, in industry current trend in the application of model checking PLC programs is using model based development tools on symbolic model checkers like NuSMV.

10 Open Problems and Research Challenges

Examining the historical development of the PLC model checking studies, we can see in Table 10 that the FBD model checking area contains the majority of the papers published in the last five years. Model checking textual PLC programs seems to saturate during 2000s although ladder diagrams being almost the same age as textual programs seem to have a constant pace of publications since they can be easily converted to propositional logic representations. The ability to use Petri Nets at a more abstract level even before the PLC program is produced, make them an area that is being studied at a constant pace

PLC prog.	Textual	LD	SFC	FBD	Petri Net	Other
- 1999	1	3	1	0	1	5
2000 - 2004	4	3	10	0	3	3
2005 - 2009	4	3	0	3	2	8
2010 -	0	2	0	5	2	3

Table 13 Number of studies related to different programming languages in five year periods

starting from 2000s. SFC based PLC model checking have its golden era in the beginning of 2000s before being replaced by FBDs, which are being widely used in industry today. Non-standard programming languages are also being constantly studied in order to overcome some difficulties like modeling PLC specific programming constructs (e.g. TONs) or to bridge the gap between widely used modeling tools (e.g. UML, LabView, etc.).

After examining the model checking studies performed in the area of PLC software verification, we shall present some important common practices that were frequently applied in the studies. After discussion of common practices we are going to present some open challenges and key points that should be considered during conducting research in the area.

10.1 Common Challenges

The challenges that were faced during specific PLC programming areas are explained in the related sections, but the common challenges that are faced during the studies in the survey can be summarized as follows:

- **State Space Explosion:** Especially textual programs possess a more granular structure, and further abstractions are needed to be applied during the automatic translation process or after the translation process manually. These abstractions aim to gather equivalent states and remove the unnecessary ones to shrink the state space by automatic conversion of the textual program. Many different techniques are applied in order to overcome state space explosion including applying further abstractions like compacting recurring place clusters inside a Petri Net into a single place.
  As mentioned, these further abstractions can be done automatically by applying a second step of automatic process during the conversion. This is often done by directly (without any abstraction) converting source code to an intermediate format using a rule based system. Successively, further abstractions are applied over the intermediate model and another conversion is performed to produce input to the target model checking tool.
  These abstractions are performed manually in some studies, but these situations negatively affected the automation of the process. Another point where manual intervention applied is over the source of PLC program. A subset of the source language instruction set is selected in almost all of the studies and additionally in most of the studies only the boolean variables

are selected to be included in the translation process. A more effort demanding solution is applied by developing specialized model checkers for the specific case.

- **Model Consistency:** The usual problem in model checking is to ensure that the built model to be checked is correct and the model represents the system consistently. For the PLC programming domain the automatic conversion is easier compared to conventional programming, because conventionally PLC program development life cycle already starts with state based representations like automata or petri nets. PLC programs using mostly primitive data types and boolean variables make the process even easier. The hard part is to model the timing constructs and reflect the real-time nature of the PLC programs. The most common solution to this problem is to apply divide and conquer strategy and reuse manually converted and heavily tested timed components of PLC programs in automating the conversion process.
- **Specifying Properties to be Checked:** A problem almost as hard as building a correct model is to correctly specify the properties to be checked using the model. Due to its low-level nature and development life cycle, PLC programs can be more easily represented with state transition systems. However when it comes to property specification, model checkers require temporal logic to be used as medium that requires expertise in formal methods and mathematical modeling area. As technology progresses, using natural language processing or conversion from a tabular format to extract specifications in LTL or CTL is expected to become more powerful by the industry. Currently it seems to be one of the most appealing research directions as well.
- **Representing PLC execution cycle:** A common challenge that was faced in most of the studies above is reflecting the PLC execution cycle to the model checking environment in a convenient way. To implement a complete system, researches have chosen to model distinct phases of the PLC execution cycle as separate modules for the model checker. Moreover, a PLC cycle sequencer module is also included in the model often to mimic the timing properties between sequences of PLC cycles. In addition to those phases, modules to model interrupts and triggers are also included in the model in some studies.
- **Modeling TONs:** Another very common challenge is the modeling of TONs (timer on-delay). TONs are used to enable an output of the PLC for a period of time when an input of TON receives true input. TONs are important for PLC programs, because they are excessively used to ensure timing properties of PLCs explicitly inside the program. A frequently applied solution in handling TONs is using a timed automata and a model checker that support real time model checking like UPPAAL.

10.2 Future Research Directions

Apart from the mostly discussed challenges and proposed solutions above, there are also less frequently discussed solutions, which can be a good point to direct future research. One of those problems is the conformance of generated models with the original program. There are studies which directly discuss this kind of problems and also some studies which propose a solution together with their model checking approach. These solutions usually involve conformance testing of the model used and a model is directly generated from the PLC program. Generating the PLC program and the model to be verified from a common ancestor model is another solution to this problem, but most of the studies still do not present sound discussions about the problem or the consistency concerns raised by this approach.

Another common drawback is the lack of performance considerations about the solution presented in the papers. Most of the time authors point to the number of defects found by their approach, but in our humble opinion this information becomes subjective if the data about size of the models being checked or the performance numbers are not present in the discussion. A serious discussion of the mentioned information about the study is needed to reason about practical aspects of the proposed approach.

Although still being tightly dependent to the improvements of model checking performance, there exist a small number of studies in model checking networked PLCs or multitasking PLCs. Even though it can be hard to overcome the state space explosion problem in such purposes it can be still interesting to push the limits by applying abstractions in this area.

We would also like to mention two more interesting commonalities in the discussed studies. From the current perspective, it can be seen that SMV and UPPAAL dominate the model checking practices on PLC programs. There can be many reasons behind this, but we believe the most effective two are tool support / ease of use and simplistic syntax that can be more easily translated from a PLC program. It is remarkable that SPIN, which is another popular model checker, is used in significantly fewer studies. Another interesting fact is that none of the discussed Petri net studies were applied on the area of railway control systems even though they are known to be applied in such systems frequently.

Most of the present challenges and future studies presented in this section is related to state space explosion problem. This situation is not surprising especially for model checking practitioners and puts the emphasis on state space reduction, being the usual suspect whenever model checking is applied in verification purposes.

Lastly, we would also like to discuss the future challenges introduced by the development of web technologies and cloud infrastructure. Latest achievements in cloud computing and Internet of Things area, awaken a demand in industrial automation on gathering and integrating information from data sources to enterprise software systems via PLCs. Many mainstream PLC hardware/-software manufacturers released web based versions of their PLC visualization

and programming software like Siemens[8], Beckhoff[9] and other software manufacturers[10][11][12][13]. PLC hardware manufacturers even make it possible to access the PLC software by web servers that runs on the PLC itself. Together with the integration issues, becoming more accessible brings security constraints into the automation control area increasing the need for verification of security requirements in PLC control and communication (Kornecki and Zalewski, 2010) (Lawton, 2011). This situation unveils a new potential to verification studies focusing on software and protocol security like Murphi (Dill, 1996) and AVISPA (Armando et al, 2005) in the next decade in PLC software verification.

11 Conclusion

Verification of PLC programs is a very widely studied area of research, and applying model checking in such purposes contains numerous studies proposing integration of a number of model checking tools over a variety of PLC programming and modeling methods. In this paper we present an overview of these methods by classifying them according to the IEC 61131 standards. Additionally, we present additional sections regarding Petri nets as being almost the most widely used modeling approach when it comes to PLC programming as well as various different non-conventional techniques proposed in the area.

During our classifications, we followed a practical approach and provided the prominent properties of the studies and the relations between these properties assuming the readers intention is to get an idea about the appropriate approach according to the area, size of the system and the type of the programming language she is planning to use in the future. We believe that our discussions are not only capable of directing the practitioners aiming to integrate model checking approaches in their software production processes but also provides an overview of the state-of-art research and open problems for the researchers interested in the area.

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