

The memory architecture has a significant effect on the flexibility and performance of a coarse-grained reconfigurable array (CGRA), which can be restrained due to configuration overhead and large latency of data transmission. Multi-context structure and data preloading method are widely used in popular CGRAs as a solution to bandwidth bottlenecks of context and data. However, these two schemes cannot balance the computing performance, area overhead, and flexibility. This paper proposed group-based context cache and multi-level data memory architectures to alleviate the bottleneck problems. The group-based context cache was designed to dynamically transfer and buffer context inside CGRA in order to relieve the off-chip memory access for contexts at runtime. The multi-level data memory was designed to add data memories to different CGRA hierarchies, which were used as data buffers for reused input data and intermediate data. The proposed memory architectures are efficient and cost-effective so that performance improvement can be achieved at the cost of minor area overhead. Experiments of H.264 video decoding program and scale invariant feature transform algorithm achieved performance improvements of 19% and 23%, respectively. Further, the complexity of the applications running on CGRA is no longer restricted by the capacity of the on-chip context memory, thereby achieving flexible configuration for CGRA. The memory architectures proposed in this paper were based on a generic CGRA architecture derived from the characteristics found in the majority of existing popular CGRAs. As such, they can be applied to universal CGRAs.

**ACM Categories & Descriptors:** B.7.1 [Integrated Circuits]: Types and Design Styles

**Keywords:** memory architecture; CGRA; context cache; cache prefetch; data memory

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## Exploring Efficiency of Ring Oscillator-Based Temperature Sensor Networks on FPGAs

Navid Rahmanikia, *Ferdowsi University of Mashhad*  
Amirali Amiri, *Technical University of Munich*  
Hamid Noori, *Ferdowsi University of Mashhad*  
Farhad Mehdipour, *Kyushu University*  
Contact: rahmanikia.navid@gmail.com

Due to technology advances and complexity of designs, thermal issue is a bottleneck in electronics designs. Various dynamic thermal management techniques have been proposed to address this issue. To effectively apply thermal management techniques, providing an accurate thermal map of chips is highly required. For this goal, a network of temperature sensors ought to be provided. There are various implementations for temperature sensors and network of sensors on Field Programmable Gate Arrays (FPGAs). This work defines and formulates four metrics and criteria, in terms of area, thermal, and power overheads and thermal map accuracy for exploring and evaluating efficiency of different implementations

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of Ring Oscillator-based Temperature Sensor (ROTS) networks on FPGAs and reports the comparison results for 12 networks with various sensor configurations. According to our metrics and experiments, the sensor that it is composed of NOT gates with open latches and RNS ring counter has lower thermal and power overheads compared to other configurations. Moreover, in this work, a new ROTS is presented that occupies 25% less resources than the most compact temperature sensor. Also, it provides 1.72 times higher sensitivity than the best sensitive ROTS design.

**ACM Categories & Descriptors:** C.4 [Performance of Systems]: Design studies, Measurement techniques, Performance attributes; B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids

**Keywords:** FPGA; Temperature; Soft-Sensor; Ring Oscillator; Network of Temperature Sensor; Exploration; Efficiency; Area Overhead; Thermal Overhead; Power Overhead; Thermal Map Accuracy

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## Formal Verification ATPG Search Engine Emulator

Gregory Ford, *IBM Microelectronics*  
Aswin Krishna, *CWRU*  
Jacob A. Abraham, *University of Texas Austin*  
Daniel G. Saab, *CWRU*  
Contact: ark70@cwru.edu

Bounded Model Checking (BMC), as a formal method of verifying VLSI circuits, shows violation of a given circuit property by finding a counter-example to the property along bounded state paths of the circuit. In this paper, we present an emulation framework for Automatic Test Pattern Generation (ATPG)-BMC model capable of checking properties on gate-level design. In our approach, counterpart to a property is mapped into a structural monitor with one output. A target fault is then injected at the monitor output, and a modified ATPG-based state justification algorithm is used to find a test for this fault which corresponds to formally establishing the property. In this paper, emulating the process of ATPG-based BMC on reconfigurable hardware is presented. The ATPG-BMC emulator achieves a speed-up over software based methods, due to the fine-grain massive parallelism inherent to hardware. As circuit sizes approach limits of even ATPG-based method feasibility, further solutions are required. In this presentation, we propose an ATPG-based algorithm for formal verification implementation on reconfigurable hardware (FPGA). This implementation is shown to have a linear relationship between the size of the circuit being verified and FPGA resource utilization. This implies a reasonable bound on the size of the implementation, as opposed to an exponential utilization explosion as circuit size increases.

This method has also been shown to be 3 orders of magnitude faster than a similar software-based approach, based on the time for solving a given ATPG problem. At the same time, though, total runtime for the FPGA emulation based implementation is significantly limited by the parts of its process still in software. Further enhancement is proposed to reduce this overhead and increase the benefit over software solvers.

**ACM Categories & Descriptors:** B.6.3 [LOGIC DESIGN]:

Design Aids - Verification, VHDL, Verilog